FRESHERS NOW

Texas Instruments Electronics Questions

Q1. Interrupt latency is the time elapsed between:

a) Occurrence of an interrupt and its detection by the CPU
b) Assertion of an interrupt and the start of the associated ISR
c) Assertion of an interrupt and the completion of the associated ISR
d) Start and completion of associated ISR

Q2. A CPU supports 250 instructions. Each instruction op-code has these fields:
- The instruction type (one among 250)
- A conditional register specification
- 3 register operands
- Addressing mode specification for both source operands.
The CPU has 16 registers and supports 5 addressing modes. What is the instruction op-code length in bits?

a) 32
b) 24
c) 30
d) 36

Q3. Consider a circuit with N logic nets. If each net can be stuck-at either values 0 and 1, in how many ways can the circuit be faulty such that only one net in it can be faulty, and such that up-to all nets in it can be faulty?

a) 2 and 2N
b) N and 2^N
c) 2N and 3^N-1
d) 2N and 3N

Q4. Which of the following statements is/are true?

I. Combinational circuits may have feedback, sequential circuits do not.

II. Combinational circuits have a memory-less property, sequential circuits do not.
III. Both combinational and sequential circuits must be controlled by an external clock.

a) I only
b) II and III only
c) I and II only
d) II only

Q5. A CPU supports 4 interrupts- I1, I2, I3 and I4. It supports priority of interrupts. Nested interrupts are allowed if later interrupt is higher priority than previous one. During a certain period of time, we observe the following sequence of entry into and exit from the interrupt service routine:
I1-start---I2-start---I2-end---I4-start---I3-start---I3-end---I4-end---I1-end
From this sequence, what can we infer about the interrupt routines?

a) I3 > I4 > I2 > I1
b) I4 > I3 > I2 > I1
c) I2 > I1; I3 > I4 > I1
d) I2 > I1, I3 > I4 > I2 > I1

Q6. For a CMOS inverter, the transition slope of Vout vs Vin DC characteristics can be increased (steeper transition) by:

a) Increasing W/L of PMOS transistor
b) Increasing W/L of NMOS transistor
c) Increasing W/L of both transistors by the same factor
d) Decreasing W/L of both transistor by the same factor

Q7. In the iterative network, the output Yn of any stage N is 1 if the total number of 1s at the inputs starting from the first stage to the N th stage is odd. (Each identical box in the iterative network has two inputs and two outputs). The optimal logic structure for the box consists of:

a) One AND gate and one NOR gate
b) One NOR gate and one NAND gate
c) Two XNOR gates
d) One XOR gate

Q8. Consider an alternate binary number representation scheme, wherein the number of ones M, in a word of N bits, is always the same. This scheme is called the M-out-of-N coding scheme. If M=N/2, and N=8, what is the efficiency of this coding scheme as against the regular binary number representation scheme? (As a hint, consider that the number of unique words represent able in the latter representation with N bits is 2^N. Hence the efficiency is 100%)

a) Close to 30%
b) Close to 50%
c) Close to 70%
d) Close to 100%

Q9. I decide to build myself a small electric kettle to boil my cup of tea. I need 200 ml of water for my cup of tea. Assuming that typical tap water temperature is 25 C and I want the water boiling in exactly one minute, then what is the wattage required for the heating element?
[Assume: Boiling point of water is 100 C, 1 Calorie (heat required to change 1 gm of water by 1 C) = 4 joules, 1 ml of water weighs 1 gm.]

a) Data given is insufficient
b) 800 W
c) 300 W
d) 1000 W
e) 250 W

Q10. Minimum number of 2-input NAND gates that will be required to implement the function: Y = AB + CD + EF is

a) 4
b) 5

c) 6
d) 7

Q11. Which of the following is true for the function (A.B + A.C + B.C)?

a) This function can glitch and can be further reduced
b) This function can neither glitch nor can be further reduced
c) This function can glitch and cannot be further reduced
d) This function cannot glitch but can be further reduced

Q12. State which of the following gate combinations does not form a universal logic set:

a) 2-input AND + 2-input OR
b) 2-to-1 multiplexer
c) 2-input XOR + inverter
d) 3-input NAND

Q13. The value (0xdeadbeef) needs to store at address 0x400. Which of the below ways will the memory look like in a big endian machine:
0x403 0x402 0x401 0x400

a) be ef de ad
b) ef be ad de
c) fe eb da ed
d) ed da eb fe

Q14. Consider a two-level memory hierarchy system M1 & M2. M1 is accessed first and on miss M2 is accessed. The access of M1 is 2 nanoseconds and the miss penalty (the time to get the data from M2 in case of a miss) is 100 nanoseconds. The probability that a valid data is found in M1 is 0.97. The average memory access time is:

a) 4.94 nanoseconds

b) 3.06 nanoseconds
c) 5.00 nanoseconds
d) 5.06 nanoseconds

Q15. For the two flip-flop configuration, what is the relationship of the output at B to the clock frequency?

a) Output frequency is 1/4th the clock frequency, with 50% duty cycle
b) Output frequency is 1/3rd the clock frequency, with 50% duty cycle
c) Output frequency is 1/4th the clock frequency, with 25% duty cycle
d) Output frequency is equal to the clock frequency

Q16. In the circuit, all the flip-flops are identical. If the set-up time is 2 ns, clock->Q delay is 3 ns and hold time is 1 ns, what is the maximum frequency of operation for the circuit?

a) 200 MHz
b) 333 MHz
c) 250 MHz
d) None of the above

Q17. In a given CPU-memory sub-system, all accesses to the memory take two cycles. Accesses to memories in two consecutive cycles can therefore result in incorrect data transfer. Which of the following access mechanisms guarantees correct data transfer?

a) A read operation followed by a write operation in the next cycle.
b) A write operation followed by a read operation in the next cycle.
c) A NOP between every successive reads & writes
d) None of the above

Q18. The maximum number of unique Boolean functions F(A,B), realizable for a two input (A,B) and single output (Z) circuit is:

a) 2
b) 6
c) 8
d) None of the above

Q19. An architecture saves 4 control registers automatically on function entry (and restores them on function return). Save of each registers costs 1 cycle (so does restore). How many cycles are spent in these tasks (save and restore) while running the following un-optimized code with n=5:

```
Void fib(int n)
{
if((n==0) || (n==1)) return 1;
return(fib(n-1) + fib(n-2));
}
```

a) 120
b) 80
c) 125
d) 128

Q20. The FSM (finite state machine) starts in state Sa, which is the reset state, and detects a particular sequence of inputs leading it to state Sc. FSMs have a few characteristics. An autonomous FSM has no inputs. For a Moore FSM, the output depends on the present state alone. For a Mealy FSM, the output depends on the present state as well as the inputs. Which of the statements best describes the FSM?

a) It has two states and is autonomous
b) The information available is insufficient
c) It is a Mealy machine with three states
d) It is a Moor machine with three states