

Section Wise - Redpine Signals Model Placement Paper

Section:1(ELECTRONICS)

Q1.Simple realization of logic gates given, we have 2 find d output?

ANS: Have to know the properties of AND,NAND, EX-OR functions

Q2.The maximum value of signed number that can be fit into 2 byte register?

ANS: We know that byte consists of 8 bits and the left most bit consist of sign hence only seven bits represent the magnitude similarly for 2 byte register d left most bit i.e.,16th bit represent sign hence the max value can be obtained by placing all 1's in remaining 15 bit positions.

Therefore d value is: $(2^{15})-1=32767$

Q3. Ideal op-amp sum was given and we have 2 find d output voltage?

ANS: It was difficult to draw d diagram i will explain d procedure so that u can b able 2 interpret d diagram easily

At terminal1: $(2-V_1)/5=(V_1-V_{out})/10$;

At terminal2: $(0-V_2)/10=(V_2-V_{out})/100$; as given it is ideal op-amp $V_1=V_2$;

By solving d above three equations we can get $V_{out}=-5.5V$

Q4.Given a series of three sources connected in a ckt with load resistor(R) and power delivered by them individually is given by 18W,50W,98W.What is the total power delivered when all the three sources are active?

ANS: $E_1^2/R=18W$;

$E_2^2/R=50W$; Equations formed by interpreting the given data

$E_3^2/R=98W$;

Hence total power delivered when all the 3 sources r active is E^2/R ;

where $E=E_1+E_2+E_3$;(as they r connected in series)

By multiplying 1st&2nd eqs we get $(E_1 \cdot E_2)/R=\sqrt{18 \cdot 50}=30W$;

By multiplying 2nd&3rd eqs we get $(E_3 \cdot E_2)/R=\sqrt{98 \cdot 50}=70W$;

By multiplying 1st&3rd eqs we get $(E_3 \cdot E_1)/R=\sqrt{18 \cdot 98}=42W$;

Therefore total power delivered is: $P=(E_1^2+E_2^2+E_3^2+2E_1E_2+2E_2E_3+2E_1E_3)/R$

$P=18+50+98+2 \cdot 30+2 \cdot 70+2 \cdot 42=68+98+60+140+84=166+200+84$

Hence total power delivered $P=450W$

Section Wise - Redpine Signals Model Placement Paper

Q5. A 26Kbyte memory, there is memory it contains 12 address lines and 4 bit data bus, the number of these type of memories required to design 26Kbyte memory?

ANS: 26K byte=26*1024=26624 bytes

Address lines=12;memory occupied= 2^{12} =4096 bytes

4 bit data bus memory can be neglected as it is very small

Hence 26624 bytes=N*4096 bytes;

=>N=26624/4096=6.5

Hence 7(6.5)type of memories r required to design 26Kbyte memory

Q6.The no of 2-input XOR gates required to design 19-input XOR gate?

Sol: Lengthy procedure.....!

Q7.This questions was given based on rising n falling edges of a flip flop?

Sol: Have a brief look on the theory of flip flops

Q8. Conversion of given multiplexers to AND gates

Q9.Convert the following:

a)73(in decimal) to binary

b)octal to binary

c)decimal to hexadecimal.....!

ANS: To convert decimal number 2 binary divide d given decimal number by 2

To convert decimal number 2 hexadecimal/octal divide d given number by 16/8

To convert binary number 2 decimal multiply d digits with powers of 2

Section:2(COMPUTING)

Q10.Simple C programs(3 questions were given)

Section Wise - Redpine Signals Model Placement Paper

Q11. Program to obtain value of 'k' and to obtain 'k' in d given program code u should have d knowledge of modular division

Eg: $16 \bmod 7$ = remainder obtained when 16 is divided by 7 i.e., 2

Q12.

$A(m,n) = n+1, \text{ if } m=0;$
 $= A(m-1, A(m,n)), \text{ if } m>0, n=0;$
 $= A(m-1, A(n,1)), \text{ if } m>0, n>0; \text{ then find } A(2,2)$

Sol: Looks simpler but takes lot of time 2 answer its based on mainly RECURSIVE function used in C language

Q13. A man walking along a railway bridge heard d whistle sound of a train when he already $5/13$ th distance of a bridge. Then he runs n can be escaped from making accident with d train. If he had ran back from there to starting point he could be escaped. If the velocity of man is 12kmph. What is velocity of man?

ANS: By given data it is clear that man has to cover total distance of d bridge and $5/13$ th distance of d bridge as he walked back. Let d distance of d bridge = 'x'

Hence total distance man has to cover = $x + (5/13)x = (18/13)x$

But train requires only 'd' distance to cover and also time taken by both must b same

=> Velocity of train = x/t ;

Velocity of man = $(18/13)x/t = 12\text{kmph}$;

=> $x/t = (12 * 13)/18 = 26/3\text{kmph}$

Q14. In a party 12 members had a board meeting and hands were shaken between them before and after d party. Therefore total no. of handshakes possible?

ANS: 1st person can shook his hand with other 11 persons => handshakes possible = 11

2nd person can shook his hand with other 10 persons => handshakes possible = 10

11th person can shake hand with 1 person only => handshakes possible = 1

Hence total no. of handshakes possible = $11 + 10 + 9 + 8 + \dots + 1 = 66$

But hands had done it twice their work in d party. Therefore total no. of handshakes possible = $2 * 66 = 132$

Section Wise - Redpine Signals Model Placement Paper

Q15. The average age of 10 members of a given committee = average age of 10 members 4 yrs. ago because older member is replaced by a younger member. What is the age difference?

ANS: Present average of ages = $(a_1 + a_2 + \dots + x)/10$ -----eq1;

Average of ages before 4 yrs ago = $(a_1 + a_2 + \dots - 9 \times 4 + y)/10$ -----eq2;

By equating eqs 1 & 2 we get

$$x = y - 36;$$

$$y - x = 36 \Rightarrow \text{the age difference is 36 yrs.!}$$

Q16. Abbreviations from CN like.....

ANS: CDMA-Code division multiple access

FTP- File transfer protocol

IEEE-Institute for electrical and electronics engineers

Digital:

It includes both STLD, VHDL and Microprocessors.

Q1) Design 3:1 multiplexer using one tri-state buffer, AND gates and NOT gates.

Q2) The no of 2-input XOR gates required to design 19-input XOR gate?

Q3) A 26Kbyte memory, there is memory it contains 12 address lines and 4 bit data bus, the number of these type of memories required to design 26Kbyte memory?

Q4) Write a VHDL or Verilog HDL code for

input: a, clock, reset

output : out is assigned to 1 when a is '1' for two clock cycles.

Q5) What is the output of following fig. 100ps is the delay for XOR gate and 50ps for AND gate. All +ve and -ve edges start at boundaries of nanoseconds. (actually the output of fig is $A(B(\text{not } C) + (\text{not } B)C)$, and the waveforms are given).

Q6) Design for which the output is 10MHz clock, input to that circuit is 30MHz. Communications:

Q7) What is Shannon's theorem?

Q8) X is Gaussianly distributed signal

a) $p(X \leq \infty) = ?$

b) X is zero mean and a unit variance random variable, then find the mean and variance of y

$$y = 2X + 5;$$

Section Wise - Redpine Signals Model Placement Paper

Q9) Because of error 000 is coded instead of 0 ,111 instead of 1. then what is the error correction and error detection capability of the system?

Q10) A deterministic signal whose pdf is given then we have to find the minimum sampling frequency needed ?